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Analysis the Effect of Subthreshold Leakage on Carry Save Adder

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Abstract: - This paper analyzes the effect of subthreshold leakage on carry save adder. When the gate to source voltage reduces and goes below the threshold voltage there is still some amount of current flow inside the circuit and that is undesired for the design. As the process technology advancing much rapidly the threshold voltage of MOS devices reduces very drastically, and it must be taken care for the low power devices since it leads to small amount of leakage current which intern increases the power consumption of the devices. Adders are the basic building blocks for any digital circuit design and it is used in almost all arithmetic calculations. The CSA proves efficient adders for Digital ICs due to its fast and accurate calculations. Hence this paper perform subthreshold analysis on CSA; and the observe results shows the total average power is nearly 4.93µW, the propagation delay for complete operation is 16.3ns and since this design uses GDI cell so there is a reduction in area with 37%.

Keywords: - Subthreshold Leakage, Gate Diffusion Input (GDI), Carry Save Adder (CSA), Leakage current, Transistor Modeling.

I. INTRODUCTION

Arithmetic circuits are basic building blocks of any digital IC design. The major functions such as addition, subtraction, multiplication, and division are used frequently in an arithmetic and logic unit of any digital IC. Since the addition and multiplication are nearly share similar functionality hence it is possible to design adders which perform both the functions very efficiently. This work design the CSA in such a way that it should consume less silicon area and perform efficient operations; to achieve this the GDI methodology is used to design the 4-bit CSA. The subthreshold leakage of CSA is measure and optimized by adjusting the MOS process parameters such as oxide thickness, channel length/width, junction depth etc. By the final optimized parameter it is also possible to analyze and reduce the leakage current of the device. The basic operation of 4-bit CSA can be understood by the following figure – 1.

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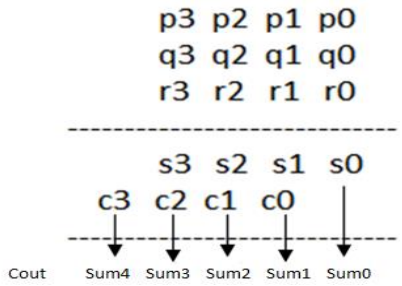

Figure – 1 Operation of 4-Bit CSA

By using CSA not only the speed of the calculation increases but also it saves the power since the carry propagation is saved between previous and next state if generated any. In this paper a 4-bit CSA is designed using GDI methodology and its operation is analyzed with respect to subthreshold leakage.

II. LITERATURE SURVEY

Tooraj Nikoubin et al [1] proposed three input xor/xnor circuit using systematic cell design methodology (SCDM) in hybrid CMOS logic style. Their design shows full swing and balanced outputs; even with supply voltage scaling they perform well and in the critical path they contain two transistors. It was proved that the proposed circuit exhibit 27% - 77% reduction in average energy delay product and also 26% - 32% improvement in area. Ramyanshu Datta et al [4] present a 4-to-2 CSA using dynamic logic and limited switch dynamic logic (LSDL) circuit family. The performance of the adder is improved as per the results. Further they used a latching element which controls the power of dynamic circuit. The LSDL methodology shows significant improvement with respect to power dissipation, leakage and area. R.Mahalakshmi and T.Sasilatha [6] made some major improvements in the design of CSA using CMOS technology. This works mainly focus on power consumption and overall chip area since for an adder structure these are the two main parameters to be concern about. Their design uses 250nm and 65nm process technology respectively, and their report shows good amount of reduction in power and area. Amuthavalli. G and Gunasundari. R [9] proposed a power aware design for ripple carry adder (RCA). The proposed circuit also helps in reducing the leakage current of the adder. This paper also analyzes the subthreshold leakage and it was shown that power due to subthreshold leakage reduces significantly as compared to conventional RCA design. They also use the multi-Threshold CMOS (MT-CMOS) in the design for maintain low power operation. M. Fonseca et al [14] present a design of a radix – 2^m hybrid array multiplier using CSA.

The proposed circuit uses partial product line in order to speed up the carry propagation along the array. Their hybrid method also improves the performance of the multiplier as it improves the speed. Their result shows the reduction in area and power dissipation as well. Ravikumar A. Javali et al [15] design CSA by using carry look ahead adder (CLA) instead of RCA, and the design approach represent the improvement in speed of the addition. The proposed design compared with respect to area, power and timings and it was shown that the CSA using CLA improves the speed of calculation with minimum effect on area and power of the design cell.

III. PROPOSED MODEL

The model for 4-bit CSA is shown in figure – 2 below.

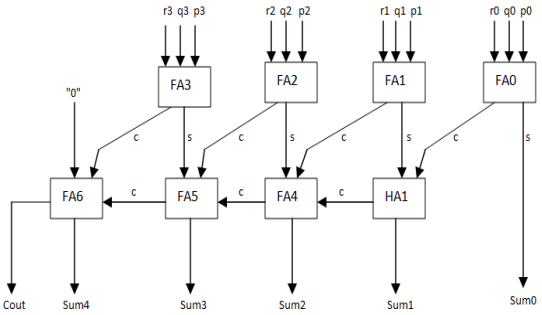

Figure – 2 Four-Bit CSA

It consists of seven full adders and single half adder. The various connections and signal flow is shown in the figure. The transistors cells are used in the design of CSA are GDI cells. GDI method is a low power design technique, by using this technique the various parameters such as power dissipation, delay, and area of digital IC is reduced much extent with very less complexity in the logic design. A 4-bit full adder using GDI cell is shown in figure – 3 below. This adder uses only 10 transistors to perform both the operations sum s well as carry.

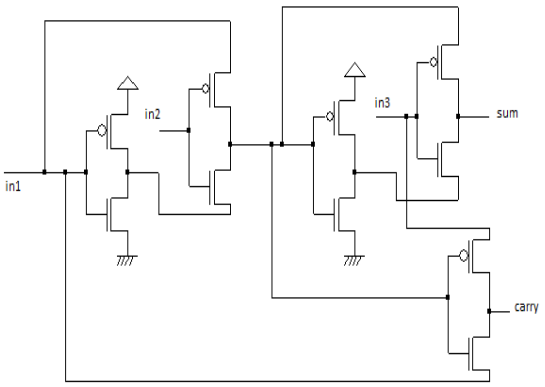

Figure – 3 One bit full adder using GDI cells.

IV. SIMULATIONS AND RESULTS

The proposed model is simulated using HSPICE and by taking 32nm standard process parameters. The functionality of the CSA is verified by writing HDL code. The various parameters related to the simulation are listed in Table – 1. The mentor graphics modelsim used for the HDL modeling of the proposed CSA. The design of CSA is done using three level hierarchy i.e. First the basic cell is designed and then using that cells the various subsystems are designed, and finally using these subsystems four bit CSA is designed. To design subsystems the GDI cells are used to reduce the power and area of the device.

Table -1Simulation Conditions

Device Name	MOS Size (W/L)
PMOS	300/32
NMOS	100/32
Supply and other Inputs	
VDD	3.2V DC
in1, in2, in3	As per the truth table (000 to 111)
Model File	32nm Standard Process Technology

The result shows the proper operation of 4-bit CSA, and the behavior of various signal involved in the design are shown below. The figure – 4 below shows the HDL model of CSA and it can be seen that CSA is working as it should.

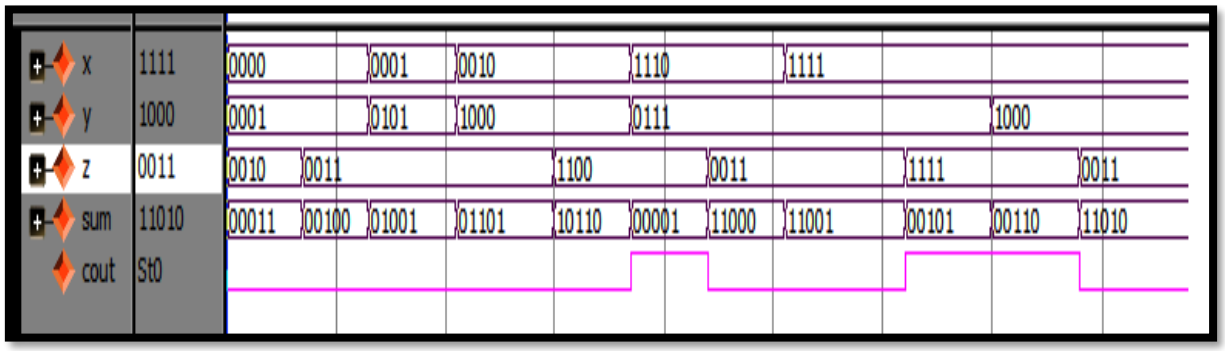

Figure – 4 HDL simulation of CSA

Figure – 5 and 6 shows the input signals to the CSA. The pulse signal is chosen for input to the CSA. The figure – 7 shows the output response of the CSA.

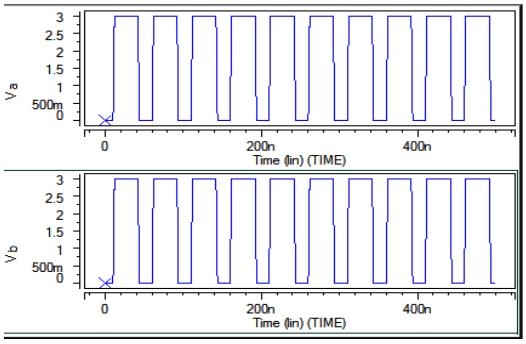

Figure – 5 Inputs to CSA

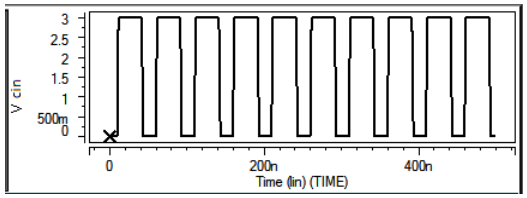

Figure – 6 Inputs to CSA

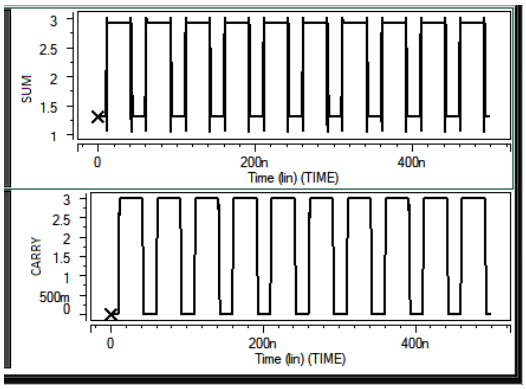

Figure – 7 Output From CSA

The figure – 8 shows the DC characteristics of the CSA. Figure – 9 and 10 shows the relationship between I_{ds} vs V_{ds} and I_{ds} vs V_{gs} respectively. According to the DC characteristic it can be concluded that the MOS is not biased from its normal operation and the subthreshold effect is also negligible so the low power operation is expected.

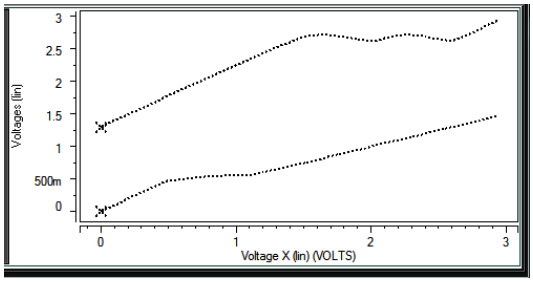

Figure – 8 DC Characterstics of CSA

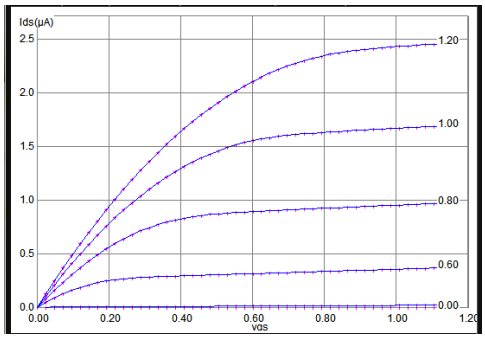

Figure – 9 Ids vs. Vds

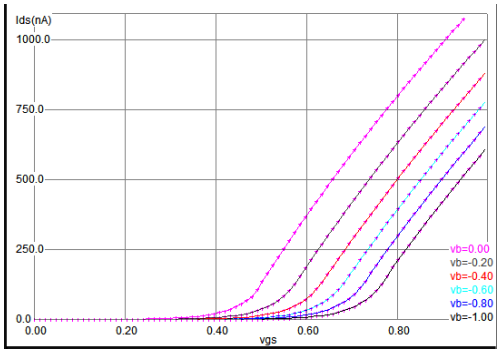

Figure – 10 Ids vs. Vgs

Figure – 11 shows the relationship between channel length and the threshold voltage, after a certain limit is reached for short channel the threshold roll off is easily seen from the graph which will help in the deciding the proper channel length of the device and it improves the device performance.

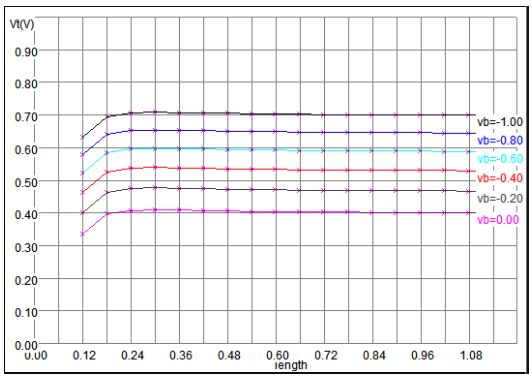

Figure – 11 V_T w.r.t Channel Length

Figure – 12 shows the two major parasitic capacitances of the one bit full adder. However these capacitances are optimized in such a way that it will not affect the circuit operation. The final optimized layout is shown in figure – 13. The table – 2 shows the optimized results.

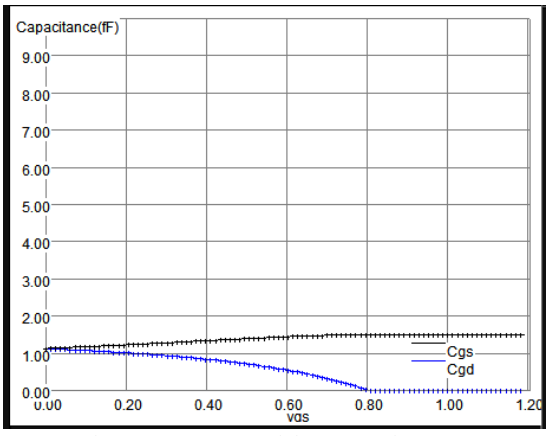

Figure – 12 Parasitic Capacitances

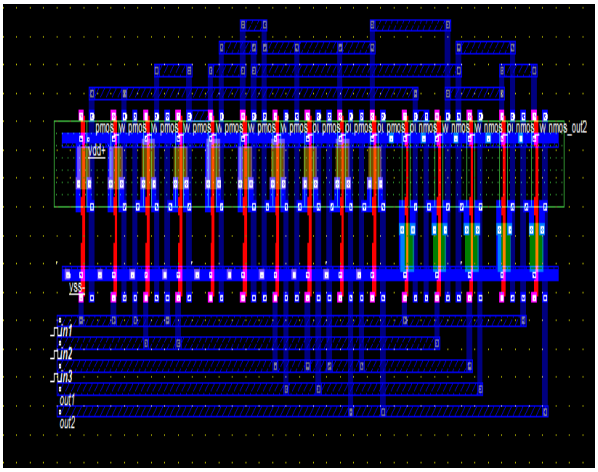

Figure – 13 Optimized Layout

Table – 2 Results

Parameters	Values
Total Average Power	4.93 µW
Cgd	0.89 fF
Cgs	1.12 fF
Propagation Delay	16.3 ns
Area Optimized (Using GDI Cell)	37%

V. CONCLUSION

This paper presents the 4-bit CSA and its working. By optimizing the process parameters it is observed that the CSA performs as it should and in subthreshold it consumes very less power since its static leakage current is reduced. The switching also reduced by reducing carries propagation to the subsequent stages which ultimately result in reduction of power dissipation of the device. The results also reveals that the GDI cell require less area as compared to conventional CMOS and it also improves the speed of operation of the device.

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